

Gyujun Jeong

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Research Profile

Georgia Tech ECE Ph.D. Student developing **applied AI for semiconductor simulation, device modeling, and EDA**. Work spans **agentic simulation and calibration workflows, GPU-accelerated physics-informed surrogate models, and AI-assisted compact/device modeling**. Demonstrated **~10,000×** acceleration of device simulation and agentic TCAD calibration with peer-reviewed publications.

Education

Georgia Institute of Technology	Atlanta, GA, USA
<i>Ph.D. in Electrical and Computer Engineering, Advisor: Prof. Shimeng Yu</i>	<i>Aug. 2025 – Present</i>
Korea Advanced Institute of Science and Technology (KAIST)	Daejeon, Korea
<i>B.S. in Electrical Engineering</i>	<i>Mar. 2018 – Feb. 2025</i>

Technical Skills

Programming and ML Systems: Python, C, CUDA, MATLAB, Tcl, Linux, Git/GitHub; PyTorch, NumPy/SciPy, pandas, scikit-learn; GPU-accelerated training, simulation-data pipelines
AI/ML Application: physics-informed neural networks, neural operators, surrogate modeling, transformers, LLM agents and agentic tool orchestration (RAG, LangChain, MCP), optimization, uncertainty and sensitivity analysis
Semiconductor, EDA, and Simulation: Synopsys Sentaurus TCAD, HSPICE; Cadence Virtuoso, Spectre; Ansys HFSS; SPICE/compact modeling, device and process simulation, synthesis, static timing analysis, design-space exploration/DTCO, advanced-node logic and memory devices

Research Experience

Georgia Institute of Technology	Atlanta, GA, USA
<i>Graduate Research Assistant, Advisor: Prof. Shimeng Yu</i>	<i>Aug. 2025 – Present</i>

- **Agentic TCAD calibration — autonomous simulation workflow.** Built an LLM agent that calibrates a *fabricated* oxide-semiconductor transistor in **five residual-guided steps** (**14.3×** **objective reduction**), replacing a multi-week expert loop: it reads measurement–TCAD residuals, retrieves candidate physics models via RAG, and applies bounded algorithmic updates through live Sentaurus runs. First-author manuscript under review at **IEEE TED** [1].
- **GPU-accelerated physics-informed surrogate — day-scale TCAD to second-scale inference.** Built a physics-informed neural operator for ferroelectric vertical-NAND charge retention that delivers **~10,000×** faster evaluation than the reference TCAD solver while preserving the governing physics constraints, converting an offline characterization study into an interactive design-space sweep; first-author **IEEE ICMC 2026 oral presentation** [2].
- **AI-assisted compact modeling for circuit-level evaluation.** Developed a physics-informed neural-network-assisted compact model that predicts process-variation behavior of non-volatile capacitive crossbar arrays from **sparse measured data**, closing the loop from device statistics to array-level circuit simulation (first-author **IEEE IRPS 2026 oral presentation** [3]); co-developed ML-assisted reliability models for oxide-channel transistors and thermally constrained on-chip power delivery [4, 5, 6].

Industry and Hardware Experience

Alsemy Inc. (SK hynix spin-off)	Seoul, Korea
<i>AI Researcher</i>	<i>Jan. 2025 – Jul. 2025</i>

- **Production AI/ML for circuit modeling.** Built neural network-based compact models (NCMs) for circuit simulation and an ML-based anomaly-detection for current–voltage measurements before they contaminate model fitting, produced a **filed patent** and shipped into the internal modeling pipeline.

Samsung Electronics, System LSI Business

Co-op Intern, Analog IP Design Team (CMOS Image Sensors)

Hwaseong, Korea

Mar. 2021 – Aug. 2021

- Improved bandgap-reference dispersion by **10%** across process corners by designing a chopper amplifier for temperature-management IP, verified in Cadence Virtuoso and Synopsys HSPICE. [post]

Georgia Tech OSPO and IBM Research AI Hardware Center

Undergraduate Research Assistant, Advisor: Dr. Kaoutar El Maghraoui

Atlanta, GA / Remote

May 2024 – Jul. 2024

- **Hardware–software co-design for AI accelerators.** Quantified how analog-inference noise and device non-idealities degrade BERT and GPT-2 accuracy using the IBM Analog Hardware Acceleration Kit, and evaluated hardware-aware training as a mitigation, linking model robustness directly to physical device behavior. [post]

Korea Advanced Institute of Science and Technology (KAIST)

Undergraduate Research Assistant, Advisor: Prof. Jaehyuk Choi

Daejeon, Korea

Jul. 2020 – Feb. 2022

- Reduced jitter-measurement delay by **25%** without a reference clock by modeling a stochastic time-to-digital-converter jitter sensor in MATLAB/Simulink, alongside phase-locked-loop design and simulation in Cadence Virtuoso [post].

Selected Publications and Patent

- [1] **G. Jeong** et al., “Agentic TCAD Calibration for Oxide Semiconductor Transistors,” **IEEE Trans. Electron Devices**, under review. [paper]
- [2] **G. Jeong** et al., “Physics-Informed AI-Accelerated Retention Analysis of Ferroelectric Vertical NAND: From Day-Scale TCAD to Second-Scale Surrogate Model,” **IEEE ICMC 2026**, oral presentation. [paper] [post]
- [3] **G. Jeong** et al., “Physics-Informed Neural Network-Assisted Compact Modeling for Process Variation in Non-Volatile Capacitive Crossbar Arrays,” **IEEE IRPS 2026**, oral presentation. [paper]
- [4] J. Kwak et al. (incl. **G. Jeong**), “Machine Learning-Assisted Compact Modeling of AC Stress-Induced Bias Temperature Instability in Top- and Bottom-Gate Oxide-Semiconductor-Channel Transistors,” **IEEE Trans. Electron Devices**, 2025. [paper]
- [5] J. Kwak et al. (incl. **G. Jeong**), “Machine Learning-Assisted Modeling of AC Stress-Induced Bias Temperature Instability in Oxide-Channel Transistors for 2T Gain Cell eDRAM,” **IEEE IRPS 2025**. [paper]
- [6] J. Kwak et al. (incl. **G. Jeong**), “Bias Temperature Instability Analysis of Oxide Power Transistors for BEOL On-Chip Voltage Converter in Thermally Constrained H3D Systems,” **IEEE IEDM 2024**. [paper]

Patent: Y. Cha, **G. Jeong**, H. Cho, “Method and Device for Removing Noise from Current–Voltage Curve Data,” South Korean Patent Application No. **10-2025-0084476**, filed June 2025.

Selected Honors

- **SK hynix Global Ph.D. Scholarship** (2026–2029) — selected multi-year graduate scholarship
- **Georgia Tech J. L. Trantham Fellowship** (2025) — awarded by Georgia Tech ECE
- **KAIST Exchange Program Scholarship** (2024) — full funding for exchange study at Georgia Tech
- **Korea National Scholarship** (2018–2024) — full undergraduate scholarship